



Figure 2 is a schematic diagram of a memory array. The array is organized into rows and columns. The rows are labeled with logical memory addresses (0xFE, 0x02, 0xFF, 0x78, 0xA0, 0xA1, 0x88, 0x70, 0x22, 0x0A, 0x09) and physical memory addresses (0xFF, 0xFE, 0xFD, 0x78, 0x77, 0x76, 0x75, 0x74, 0x02, 0x01, 0x00). The columns are labeled with physical memory addresses (0xFF, 0xFE, 0xFD, 0x78, 0x77, 0x76, 0x75, 0x74, 0x02, 0x01, 0x00). The array is divided into three sections: a top section (rows 0xFE to 0xFF), a middle section (rows 0x78 to 0x70), and a bottom section (rows 0x22 to 0x09). The top section is labeled 30, the middle section is labeled 32, and the bottom section is labeled 34. The array is organized into rows and columns. The rows are labeled with logical memory addresses (0xFE, 0x02, 0xFF, 0x78, 0xA0, 0xA1, 0x88, 0x70, 0x22, 0x0A, 0x09) and physical memory addresses (0xFF, 0xFE, 0xFD, 0x78, 0x77, 0x76, 0x75, 0x74, 0x02, 0x01, 0x00). The columns are labeled with physical memory addresses (0xFF, 0xFE, 0xFD, 0x78, 0x77, 0x76, 0x75, 0x74, 0x02, 0x01, 0x00). The array is divided into three sections: a top section (rows 0xFE to 0xFF), a middle section (rows 0x78 to 0x70), and a bottom section (rows 0x22 to 0x09). The top section is labeled 30, the middle section is labeled 32, and the bottom section is labeled 34.

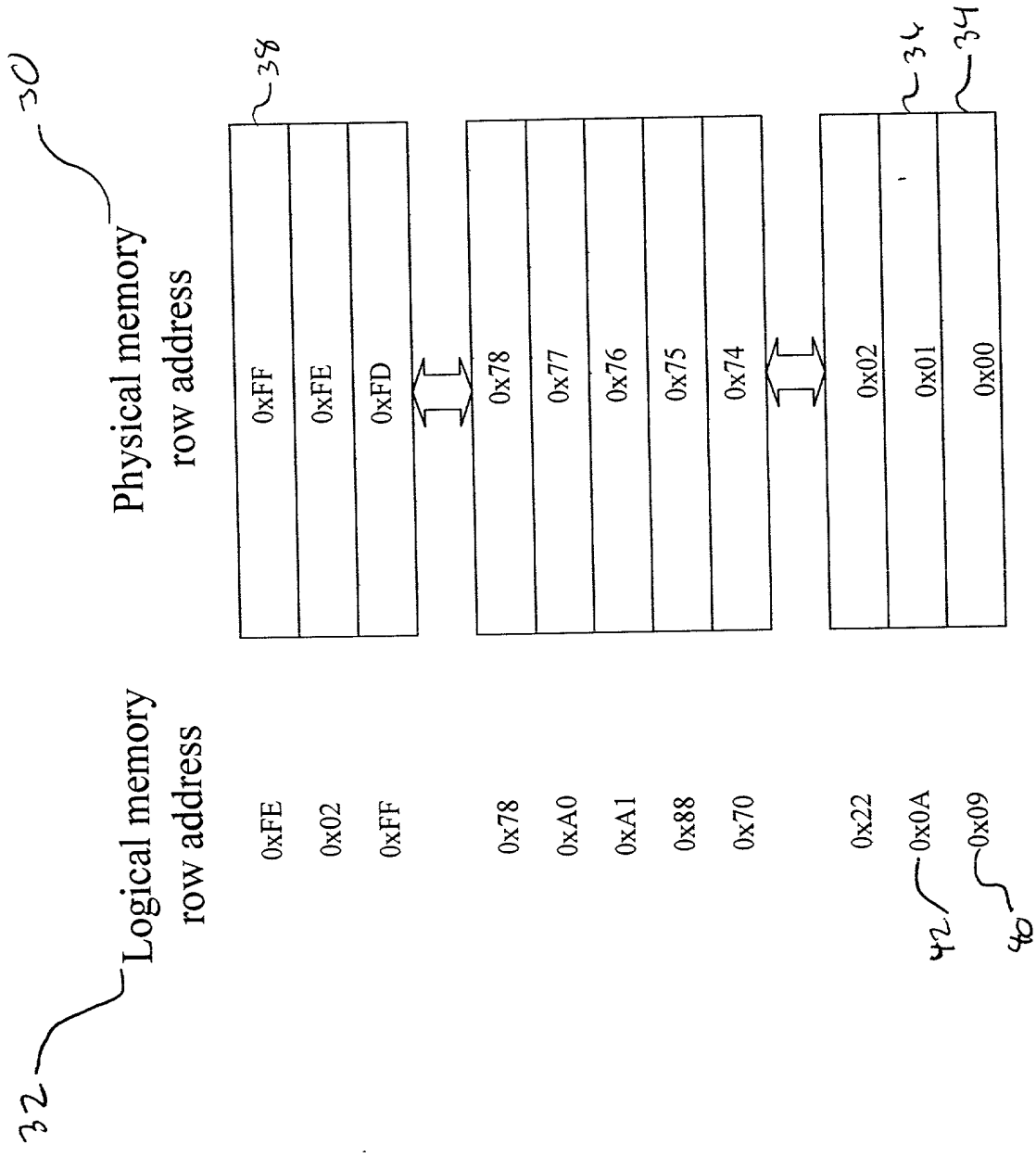


Figure 2

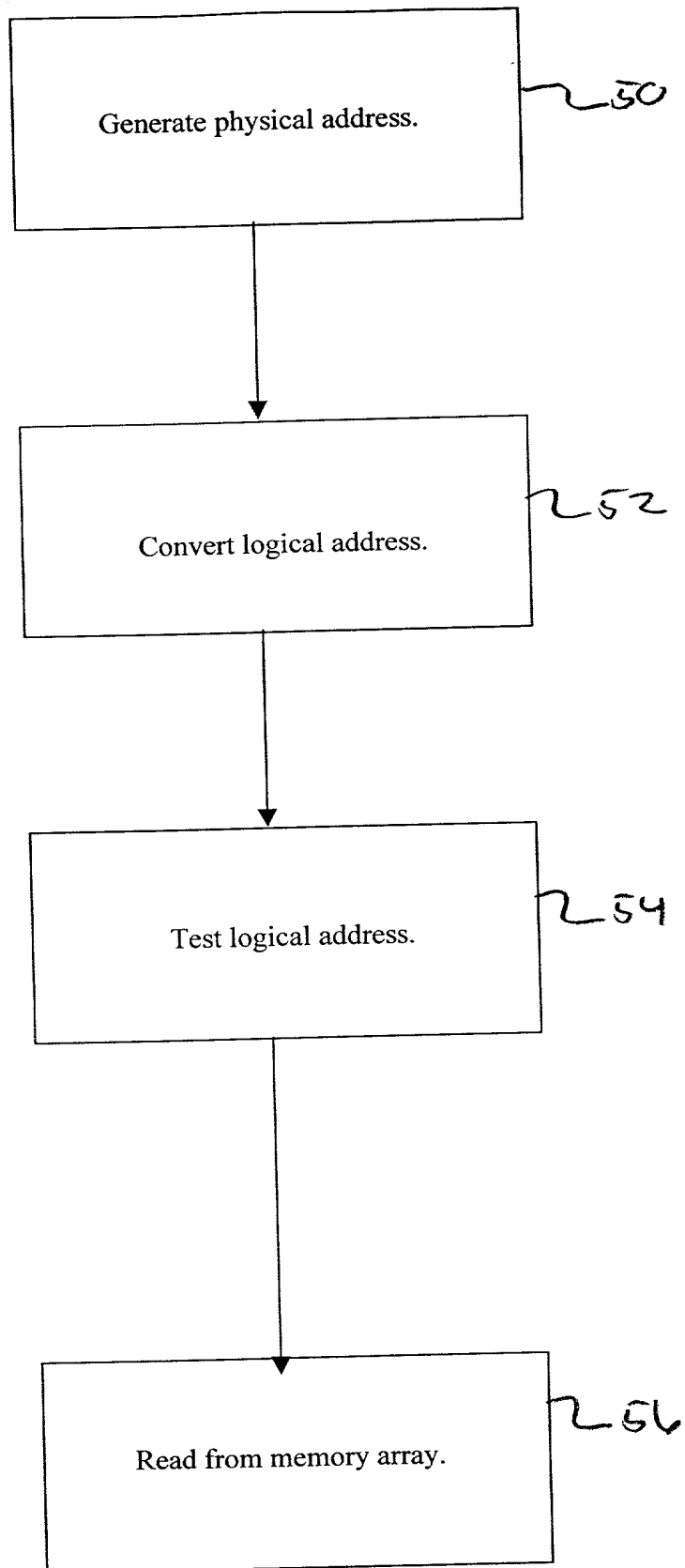


Figure 3